

ABSTRACT

A process for forming a transistor having a gate width of less than 70 nm is disclosed herein. The process includes E-beam radiation a gate patterned on a photoresist layer, trimming the gate patterned on the photoresist layer, and
5 etching the gate patterned on the photoresist layer to a polysilicon layer disposed below the photoresist layer. The gate pattern is E-beam irradiated by an electron beam.

1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25